In the Claims

1. (presently amended) A method of operating an electronic device having a plurality of memory ~~devices~~ dice, each memory ~~device~~ die having at least two sub-arrays therein, the method comprising:

individually addressing each sub-array of each said memory ~~device~~ die by communicating an address ~~specific~~ to that sub-array across an address bus coupled to all said memory ~~devices~~ dice, and by individually selecting said individual memory ~~device~~ die from among said plurality of memory ~~devices~~ dice, while the remainder of said memory dice except said individual memory die remain in a standby mode.

2. (presently amended) The method of claim 1, wherein said plurality of memory ~~devices~~ dice are formed as a part of a memory module.

3. (presently amended) The ~~memory device~~ method of claim 1, wherein said electronic device comprises a computer.

4. (presently amended) A method of operating an electronic device having a plurality of memory ~~devices~~ dice associated therewith, each memory ~~device~~ die having at least two sub-arrays therein, the method comprising:

~~individually selecting at least one individual memory device from among said plurality of memory devices; and~~

~~individually~~ addressing ~~a~~ every ~~selected~~ sub-array of said selected memory ~~device~~ die by communicating an address specific to a memory cell of each ~~that~~ sub-array across an address bus coupled to each memory ~~device~~ die of said plurality of memory ~~devices to~~ dice; and

accessing ~~a~~ one memory cell in every ~~said selected~~ sub-array of only said selected memory die.

5. (presently amended) The method of claim 4, further comprising maintaining at least one memory ~~device~~ die of said plurality of ~~devices~~ dice in a standby mode, while accessing said memory cell in said selected sub-array.

6. (presently amended) The method of claim 4, wherein said individual selection of said at least one individual memory ~~device~~ die comprises decoding a plurality of activation signals to determine the memory ~~device~~ die to be individually selected.

7. (presently amended) The method of claim 4, further comprising:

~~selecting~~ addressing a number of said memory ~~devices~~ dice from said plurality of memory ~~devices~~ dice; and

enabling only one die from said plurality of memory dice to access~~ing~~ a number of data bits from only said selected memory die ~~, wherein said number of data bits accessed is greater than said number of memory devices selected~~.

8. (presently amended) A method of configuring an electronic system having a plurality of memory devices therein, comprising:

providing a plurality of memory ~~devices~~ dice, each memory ~~device~~ die having a plurality of ~~banks~~ sub-arrays therein;

coupling a plurality of data lines to each memory ~~device~~ die, with each data line coupled to only one ~~bank~~ sub-array in each memory ~~device~~ die;

coupling an address bus to each memory ~~device~~ die, said address bus configured to allow access of ~~a~~ one memory cell in ~~any bank~~ each sub-array of said plurality of ~~banks~~ sub-arrays in each die of said plurality of dice ~~said memory device~~; and

providing at least one chip select mechanism to facilitate individual selection of each memory ~~device~~ die, said system configured to allow fewer than all of said plurality of memory ~~devices~~ dice to be selected and activated, while the remaining memory ~~devices~~ dice of said plurality of memory ~~devices~~ dice are unselected and in a low power mode.

9. (presently amended) The method of claim 8 wherein said memory ~~devices~~ dice are physically coupled to a memory module.

10. (original) The method of claim 8 wherein said electronic system comprises a computer.

11. (new) The method of claim 1 further comprising providing a memory die having only one sub-array which supplies a parity bit.

12. (new) The method of claim 4 further comprising providing a memory die having only one sub-array which supplies a parity bit.

13. (new) The method of claim 8 further comprising providing a memory die having only one sub-array which supplies a parity bit.